SPECIFICATION AMENDMENTS

Page 1, please replace the paragraphs at lines 15 to 25 with the following text:

The APS comprises per pixel a photodiode, a MOS switch, and an amplifying circuit to amplify a signal from the photodiode and has a lot of advantages such that "XY addressing" and "integration of a sensor and a signal processing circuit into one chip" are possible.

Moreover, in recent years, the APS is attracting attention due to improvement in ~~microfablication~~ microfabrication technology for MOS transistors and increased requirement for "integration of a sensor and a signal processing circuit into one chip" and "reduction in power consumption," etc.

Pages 5 and 6, please amend the paragraph bridging pages 5 and 6 to read as follows:

In order to read out signals, at least operations to be implemented during periods A2 to D2 are implemented as shown in FIG. 30. Reference character ϕ15 denotes a controlling pulse applied via a reset switch line 5 to an electrode 15 connected thereto while reference character ϕ17 denotes a controlling pulse applied via a selecting switch line 7 to an electrode 17 connected thereto, reference character ϕ16 denotes a controlling pulse via a ~~reset~~ transfer switch line 6 to an electrode 16 connected thereto, reference character ϕ22 denotes a controlling pulse of a switch 22, and reference character ϕ24 denotes a controlling pulse of a switch 24, respectively.

Page 18 and 19, please amend the paragraph at lines 11-16 and the paragraphs bridging pages 19 and 19 to read as follows:

During the period A1 shown in FIG. 5, the switch Q5 is turned on with the control pulse VR and a voltage of a high level is applied to the signal output line 58. Thus, the input terminals of the source followers of all the ~~unite~~ unit cells are reset to the reset voltage via the reset switch Q2.

Next, the switch Q5 is turned off with the control pulse VR. Moreover, a high level voltage is applied to a selecting switch line 7 of the preceding row with a control pulse S1 so that the selecting switch Q4 of the preceding row is turned on. Switches ~~S2~~ 22 of all the columns are turned on and then off with the control pulse 22 and the output voltages thereof are written into the holding capacities 23 for noise signals (period B1). At this time, the gate voltage of the reset switch Q2 will be lowered by a voltage corresponding to the threshold value voltage than the source voltage of the reset switch Q2 so that the reset switch Q2 will be turned off.

Page 19, please amend the paragraph at lines 12-16 to read as follows:

During the period D1, the switch ~~S1~~ 24 is turned on and then off with the control pulse ϕ24 so that the optical signal output containing the noise signal component is written in the holding capacity 25 for optical signals.

Page 33, please amend the paragraph at lines 7-25 to read as follows:

Next, the switch Q5 is turned off with a control pulse ϕVR. Moreover, with a control pulse ϕS1, a high level voltage is applied to the selecting switch line 67 of the (n-1)-th row to turn on the selecting switch Q4(n-1). As a consequence hereof, the signal output line 58 is lowered to a low voltage by a constant-current load 21 of the source follower. At this time, the source follower operates and a voltage appearing in the signal output line 58 will become a voltage that has dropped from the reset voltage by a voltage equivalent to the threshold value voltage. The switch ~~S2~~ 22 is turned on and then off with a control pulse ϕ22, and the output voltage is written into a holding capacity 23 for noise signals as shown in FIG. 29 (period B1). At this time, the gate voltage of the reset switch Q2 will become lower by a voltage equivalent to the threshold value voltage than the source voltage of the reset switch Q2, so that the reset switch Q2 will be turned off.